UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/858,410	05/16/2001	Dave MacAdam	5646-52	1980

20792 7590 05/31/2006

MYERS BIGEL SIBLEY & SAJOVEC
PO BOX 37428
RALEIGH, NC 27627

EXAMINER	
ELALLAM, AHMED	
ART UNIT	**PAPER NUMBER**
2616	

DATE MAILED: 05/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/858,410	MACADAM ET AL.	
	Examiner	Art Unit	
	AHMED ELALLAM	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,16 and 18-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,16 and 18-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This communication is responsive to Amendment filed on 1/24/2006.

Claims 1-12,16, 18, and 19-29 are pending.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. Claims 1-12, 16,18-29 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Regarding claims 1-12, 16, 18-29, the specification does not describe the frame offset(s) and or delay(s) with respect to a given reference. More specifically, it is not clear to what reference the delay(s) and/or offset(s) are determined.

Regarding claims 16 and 18, the specification does the specification doesn't adequately describe the retaining of frame **delay/offset** bytes by the first storage device, with each of the frame **offset/delay** bytes **identifying a frame delay or frame offset,** and the second storage device which is at least temporarily retains data that identifies presence of an unacceptable frame **delay/offset** within first storage device.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 16, 23, 27, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art, specification pages 1-2 and figure 1-2 in view of Koenig et al, US 6,879,603 and further in view of Graves et al, US 4,698,806. Hereinafter referred to as APA and Koenig and Graves respectively.

Regarding claim 1, the figure 1 of prior art shows a time-slot interchange switch (TIS) comprising an internal frame alignment counter 12 in combination with internal frame alignment register 14 for determining frame offset of a received frames, see page 1, lines 7-15, and internal frame offset 18 for storing the frame offsets, and a temporary register 24 for identifying presence of unacceptable frame offsets (see figure 1 and 2) external to the TSI switch and for temporary storage of frame offset bits that can be provided as program data to the internal frame offset register 18, see page 2, lines 15-24. (Examiner interpreted the combination of both the internal circuitry and external circuitry of prior art (figure 1) as being the claimed an internal frame alignment measurement and programming circuit).

Regarding claim 16, APA discloses time-slot interchange switch comprising:

Conventional table retaining frame delay/offset bytes with each of the frame offset/delay bytes identifying a frame delay or frame offset associated with a respective multi-frame data stream received by the switch, see figure 2, specification page 7, lines 30-31 and page 8, line1, and lines 28-31, page 9, lines 1-4. (Claimed a first storage device that is disposed internal to said switch and retains frame delay/offset bytes, with each of the frame offset/delay bytes identifying a frame delay or frame offset associated with a respective multi-frame data stream received by said switch).

Temporary register 24 for identifying presence of unacceptable frame offsets (see figure 1 and 2) external to the TSI switch and for temporary storage of frame offset bits that can be provided as program data to the internal frame offset register 18, see page 2, lines 15-24.

Regarding claim 23, the figure 1 of prior art shows a time-slot interchange switch (TIS) comprising an internal frame alignment counter 12 in combination with internal frame alignment register 14 for determining frame offset of a received frames, see page 1, lines 7-15, and internal frame offset for storing the frame offsets, and a temporary register 24 for identifying presence of unacceptable frame offsets (see figure 1 and 2) external to the TSI switch and for temporary storage of the frame offset bits that can be provided as program data to the internal frame offset register 18, see page 2, lines 15-24. APA further discloses a user reads out the count signal and may use conventional delay limit check circuitry 20 to determine whether the frame delay for a given multi-frame data stream exceeds the rating of the switch, see page 2, lines 9-14.

Regarding claim 27, the figure 1 of prior art shows a time-slot interchange switch (TIS) comprising an internal frame alignment counter 12 in combination with internal frame alignment register 14 for determining frame delay of a received frames, see page 1, lines 7-15, and internal frame offset for storing the frame offsets, and a temporary register 24 for identifying presence of unacceptable frame offsets (see figure 1 and 2) "external to the TSI switch" and for temporary storage of frame offset bits that can be provided as program data to the internal frame offset register 18, see page 2, lines 15-24. The prior art further discloses using conventional delay limit check circuitry 20 to determine whether the frame delay for a given multi-frame data stream exceeds the rating of the switch, see page 2, lines 10-12. (Claimed determines and stores a first frame delay associated with a first multi-frame data stream received by the switch in a frame delay register associated , and at least retain data that identifies presence of an unacceptable frame delay in the internal frame delay register).

As to claims 1, 16, 23, and 27:

The difference between claims 1, 16, 23 and 27 and the prior art is that APA identify the presence and not the location of an unacceptable offset(s) in the internal frame offset register, and the temporary register is external instead of being internal to the TSI switch.

However Koenig discloses implementing a TSI within a DSP processor. It would have been obvious to an ordinary person of skill in the art at the time the invention was made to have the external circuitry of the prior art implemented using a single DSP

based TSI switch as taught by Koenig so that both internal and external circuitry of prior art can be integrated. The advantage would be the ability to provide flexibility in design and reduction in space of the TSI switch.

Further, Graves discloses producing an address, for storage of each byte of each tributary in a memory, from the current count and the stored value representing the offset for the respective tributary, see column 2, lines 19-23. (Claimed temporary retaining data that identify a location of corresponding offset).

It would have been obvious to an ordinary person of skill in the art at the time the invention was made to implement the offsets address indication as taught by Graves in the system of Koenig in view of APA so that address based offsets location can be determined. The advantage would be a fast access to any specific frame offset by a user of APA. In addition frame alignment function can also incorporate a time switching function. See Graves, Abstract, and column 2, lines 30-32.

Regarding claims 2 and 28, APA discloses a table (figure 2) implemented by internal frame register 18 for retaining data that is accessible by a user, see figure2, page 2, lines 9-14. (Examiner interpreted the function provided by the claimed error code register of being the same as the internal frame offset register 18)

Regarding claims 3 and 4, APA discloses internal frame alignment counter 12 that determine frame delay associated with a first multi-frame data stream, and offset conversion circuit 16 that converts the first delay into a first frame offset.

Response to Arguments

3. Applicant's arguments filed on 01/24/2006 have been fully considered but they are not persuasive.

35 USC § 112 second paragraph:

Amendment to claims 19 and 20 overcame the 112 2nd paragraph rejections.

35 USC § 112 first paragraph:

In response to Examiner's indication that the specification does not describe the frame offset(s) and or delay(s) with respect to a given reference. Applicants stated that the *"calculation of delay and frame offsets are conventional and well known to those skilled in the art (see, e.g., FIG. 2, which illustrates how the frame delay bits relate to the clock period shift). In particular, the text at p. 7, line 15 - p. 8, line 15 of the specification explain how a "count" is maintained of how many clock pulses occur between receipt of the FOi signal and receipt of the frame evaluation (FE) signal for a respective data stream under evaluation. This number of clock pulses represents a degree to which the respective data stream is delayed relative to the FOi signal. As understood by those skilled in the art, this well known delay value represents a "frame offset" for a respective data stream".* Emphasis added.

Examiner reviewed the passage relied upon *"p. 7, line 15 - p. 8, line 15"* and found that such passage does clearly describe the delay and frame offset of being conventional as alleged by Applicants. In particular, Applicants assertion that *a "count" is maintained of how many clock pulses occur between receipt of the FOi signal and*

receipt of the frame evaluation (FE) signal for a respective data stream under evaluation" doesn't explain the claimed determination or the measurement of frame offset associated with received multi-frame data stream", for example, on page 7, lines 21-24, it is recited that "The delays associated with receiving a frame evaluation (FE) pulse from an external device may be caused by variable path lengths and variable path serial backplanes". Such statement is contradictory with the illustrations of figures 3, 5-7 in which the FE signal is indicated of being generated by the switch itself and not coming from an external device. Many issues with regard to the description are still unresolved, to name of few for example, the clear meaning of FOi signal (frame output signal), is it a signal that indicate a frame being output from receive buffer for example? Does the FE represent specific bits of a frame? Or an internal signal generated when a specific pattern is detected in the received frame? Examiner concludes that since the FOi and the FE are not clearly explained, the resulting delay and offset from these values is a clear basis for the lack of description of the claimed delay and /or offset of a frame of received multi-frame data stream. Applicants did not provide any concrete evidence to support the alleged offsets and delays being conventional and that such allegations are considered to be Applicant's own conclusion.

Claims 16 and 18:

Applicants pointed out to the first storage device being a register having M row of storage unit, and the second storage device of being retaining "an M-bit error code". Further Applicants referred to unit 118 in figure 3 of being the first device and unit 114 of

being the second device. However, the claimed **delay/offset** bytes retained by the first register for identifying a frame delay **or** frame offset is not clearly described. The first storage device is shown in figure 3 of having only an indication of frame offsets bytes and not frame delay bytes. Therefore, the "frame delay/offset bytes" is understood to only identify frame offsets and not frame offsets or frame delays. Examiner maintains that the features claimed with regard to the **delay/offset** are not adequately described.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Adam et al, US 6,781,984.

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AHMED ELALLAM whose telephone number is (571) 272-3097. The examiner can normally be reached on 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, To Doris can be reached on (571) 272-7629. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AHMED ELALLAM
Examiner
Art Unit 2616
5/22/06

KEVIN C. HARPER
PATENT EXAMINER